ABSTRACT OF THE DISCLOSURE

A non-blocking load buffer is provided for use in a high-speed microprocessor and memory system. The non-blocking load buffer interfaces a high-speed processor/cache bus, which connects a processor and a cache to the non-blocking load buffer, with a lower speed peripheral bus, which connects to peripheral devices. The non-blocking load buffer allows data to be retrieved from relatively low bandwidth peripheral devices directly from programmed I/O of the processor at the maximum rate of the peripherals so that the data may be processed and stored without unnecessarily idling the processor. I/O requests from several processors within a multiprocessor may simultaneously be buffered so that a plurality of non-blocking loads may be processed during the latency period of the device. As a result, a continuous maximum throughput from multiple I/O devices by the programmed I/O of the processor is achieved and the time required for completing tasks and processing data may be reduced. Also, a multiple priority non-blocking load buffer is provided for serving a multiprocessor running real-time processes of varying deadlines by prioritization-based scheduling of memory and peripheral accesses.

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